



CMP's Semiconductor Insights Recognizes Micron's 78nm 1Gb DDR3 as Most Innovative DRAM

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San Francisco, CA , Wednesday, September 26, 2007 – CMP's Semiconductor Insights (SI), the leader in technical and patent analyses of integrated circuits and electronic systems, today announced that it has awarded Micron's 78nm 1Gb DDR3 the 2007 INSIGHT Award for Most Innovative DRAM. The INSIGHT Awards program, produced in conjunction with Semico and EE Times, recognizes corporate and individual achievements in technology.

The INSIGHT Awards honor innovations in eight categories including DRAM, Non-Volatile Memory, RF IC, Baseband and/or Applications Processor, Process Technology, Display Driver and the Dr. Doug Smeaton Innovation Award. SI nominates a majority of the devices, but also considers vendor-submitted nominations. The awards are selected by Semico president Jim Feldham and EE Times Executive Editor, Patrick Mannion, and they are chaired by Chief Technology Officer, Edward Keyes.

"Micron's first production foray into the emerging DDR3 market pushes advanced process lithography," stated Young Choi, SI's Technology Manager – Memory. "This is also the only 6F² DDR3 design that we have analyzed, giving Micron an impressive die size."

The 6F² cell implementation reduces the Micron die's chip size by 24 percent compared with the competing DDR3 solution from Samsung, which implements an 8F² design. The technology offers many advantages over 8F² layout implemented by competitors. The 6F² cell size reduces array area and thus reduces manufacturing costs. This is extremely important in the emerging DDR3 market, where uptake will take place when price parity with DDR2 solutions is met. Despite the advantages of 6F² technology there are several design challenges, including array architecture, wordline coupling, and sense amplifier layout that has prevented many from pursuing the technology.

"We are pleased that our innovations in developing next-generation DRAM have been recognized by Semiconductor Insights' 2007 INSIGHT Award program," said John Schreck, Micron vice president of DRAM Development. "We have achieved great technical strides with our 1Gb DDR3 DRAM including its increased speeds, low power and small die size. All enabled by our mass production 78nm 6F² process and other design innovations."

Recent SI analysis of competing DDR3 devices positions Micron favorably in the market. "By using a 78nm process and 6F² technology, Micron achieves the smallest cell size of any DRAM device analyzed to date at only 0.0365µm²," added Choi. "The Metal-Insulator-Metal (MIM) capacitor cell design and recessed-channel access transistor provide small wordline and bitline pitch measurements of 156nm each."

Additional Information:

- Image: [Micron's 1 Gb DDR3 die photo](#)
- About: [Micron's 1G 78nm DDR3 SDRAM](#)
- EETimes Article: [1-Gbit DDR3 SDRAMs square off](#)

About Semiconductor Insights — A CMP Company

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