



ONFI Introduces New 2.3 Specification With ECC Offload Functionality

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SANTA CLARA, Calif., Aug 16, 2010 (GlobeNewswire via COMTEX News Network) -- The Open NAND Flash Interface (ONFI) Working Group, the organization dedicated to simplifying integration of NAND Flash memory into consumer electronic devices, computing platforms, and industrial systems, today introduced its new ONFI 2.3 specification, which includes the EZ-NAND protocol. EZ-NAND, which stands for error correction code (ECC) Zero NAND, was designed to remove the burden of the host controller to keep pace with the fast changing ECC requirements of NAND technology.

In today's NAND implementations, the host controller must assume responsibility for all NAND management functions, including block management, wear leveling, and ECC. With ECC being almost solely dependent on the NAND technology and not the system, EZ-NAND will alleviate the issue of controller manufacturers having to implement and keep up with the rapidly changing NAND ECC requirements.

"ONFI's new 2.3 specification with its EZ-NAND protocol provides the ultimate win-win scenario," said Kevin Kilbuck, chair of the ONFI marketing committee and director of strategic NAND marketing for Micron. "NAND continues to scale at its own technology cadence while host controllers can be optimized for a variety of applications, free of ECC management issues. This can enable longer platform cycles for customers and potentially lower system cost."

"EZ-NAND enables faster adoption of new technologies by having NAND providers develop standard solutions to vendor and lithography specific challenges like ECC," said Robert Selinger, senior director, SSD research and development, SanDisk. "By helping to design this new standard, we produced a specification that offers maximum performance while preserving the external host controller's ability to offer its own unique capabilities."

The EZ-NAND packages and electrical interfaces are the same as defined in the ONFI 2.2 specification. ONFI 2.3 includes some minor command set changes to execute the optional ECC off-load protocol, with the goal being to keep ONFI 2.3 as compatible as possible with today's implementations.

Separately, ONFI also announced today its continued progress on the ONFI 3.0 specification with a draft revision currently under review by the ONFI membership. The ONFI 3.0 specification, which will reach speeds of 400MT/s, is expected to be ratified in the fourth quarter of 2010. ONFI is collaborating with JEDEC to define a 400MT/sec interface, ultimately providing a single, industry-standard, high-speed NAND interface.

Visit ONFI at the Flash Memory Summit this week at the Santa Clara Convention Center, booth #215.

About ONFI

The ONFI Working Group is dedicated to simplifying integration of NAND Flash memory into consumer electronics (CE) applications and computing platforms. Before the advancements made by the working group, use of NAND Flash in these end-use applications was hampered by the lack of sufficient standardization. To support a new NAND Flash component on a platform, host software and hardware changes were often required. Implementing these changes was extremely costly due to the new testing cycle required -- which led to slower rates of adoption for new NAND Flash components. ONFI aims to remedy that problem and speed time to market for NAND Flash based applications.

The ONFI Working Group was formed in May 2006 and currently has more than 90 member companies. ONFI's founding companies include Hynix Semiconductor, Intel Corporation, Micron Technology, Inc., Phison Electronics Corporation, SanDisk, Sony Corporation, and Spansion.

Please visit www.ONFI.org for more information on the initiative and how to become a contributor.

The ONFI logo is available at <http://www.globenewswire.com/newsroom/prs/?pkgid=6949>

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