



Micron DDR5 Memory Now Available for 4th Gen AMD EPYC Processors

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The combination scales up to 2X the performance for select HPC memory-bound workloads

BOISE, Idaho, Nov. 10, 2022 (GLOBE NEWSWIRE) -- Micron Technology, Inc., (Nasdaq: MU) today announced availability of [DDR5 memory](#) for the data center that is validated for the new AMD EPYC™ 9004 Series processors. As modern servers pack more processing cores into CPUs, the memory bandwidth per CPU core has been decreasing. Micron DDR5 alleviates this bottleneck by providing higher bandwidth compared to previous generations, enabling increased reliability and scaling. The combination of 4th Gen AMD EPYC processors and Micron DDR5 delivers up to two times memory bandwidth on the STREAM benchmark and up to two times performance improvement on select HPC workloads such as computational fluid dynamics (OpenFOAM), Weather Research and Forecasting (WRF) modeling and CP2K molecular dynamics.

"Micron continues to lead the industry transition to DDR5," said Raj Hazra, senior vice president and general manager of Micron's Compute and Networking Business Unit. "Algorithms that are increasingly memory-bound need far greater memory performance and reliability to extract insights from huge volumes of data. DDR5 provides the next significant advancement in system memory capabilities required to enable these algorithms, thereby continuing to advance the value of next generation data center infrastructure."

"4th Gen AMD EPYC processors continue to raise the bar for workload performance in the modern data center while simultaneously delivering exceptional energy efficiency. 4th Gen AMD EPYC processors will transform our customers' data center operations by accelerating time to value, driving lower total cost of ownership, and helping enterprises to address their sustainability goals," said Ram Peddibhotla, corporate vice president, EPYC product management, AMD.

Micron compared the performance of the STREAM benchmark on a single 4th Gen AMD EPYC processor system populated with Micron DDR5 at 4800 MT/s to a 3rd Gen AMD EPYC processor system and Micron DDR4 at 3200 MT/s. With the 4th Gen AMD EPYC processor system, Micron achieved a peak memory bandwidth of 378 GB/s per socket compared to 189 GB/s with 3rd Gen AMD EPYC processor system. This resulted in a two times increase in system memory bandwidth.

In partnership with AMD, Micron evaluated three HPC workloads (OpenFOAM, WRF and CP2K) on 3rd Gen AMD EPYC processors with Micron DDR4 and 4th Gen AMD EPYC processors with Micron DDR5. The 4th Gen AMD EPYC processor platform with Micron DDR5 improved the performance of OpenFOAM by 2.4 times, WRF by 2.1 times and CP2K by 2.03 times.

"The continued growth of modeling & simulation, and machine learning workloads in HPC and AI means that our customers are demanding memory solutions that maximize effective bandwidth. Our collaboration with Micron throughout the development and validation phase, with these performance-intensive workloads in mind, allows us to deliver next-generation platforms with a new era in memory performance accelerated by DDR5," said Scott Tease, vice president of HPC & AI, Lenovo Infrastructure Solutions Group.

Micron has played a pivotal role in JEDEC's creation of DDR5 memory specifications and was one of the first to sample DDR5 to customers. Micron's Technology Enablement Program (TEP), the first of its kind in the industry, gave system designers early access to key internal resources to assist their DDR5 validation and qualification processes. Micron is committed to partnering across the ecosystem and will continue to invest in our leadership technology and product roadmaps.

Resources -

- [Micron Data Center Solutions](#)
- [HPC Workload Performance Blog](#)
- [DDR5 Delivers Next-Gen Data Center Performance](#)
- [Micron Chips Out Loud Podcast](#)
- [Micron TEP Program](#)

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Micron Media Relations Contact Kelly Sasso Micron Technology, Inc. +1 (208) 240-3410 ksasso@micron.com Micron Investor Relations Contact Farhan Ahmad Micron Technology, Inc. +1 (408) 834-1927 farhanahmad@micron.com