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Hybrid Memory Cube Consortium Advances Hybrid Memory Cube Performance and Industry Adoption With Release of New Specification

SAN JOSE, Calif. and BOISE, Idaho, Nov. 19, 2014 (GLOBE NEWSWIRE) -- The Hybrid Memory Cube Consortium (HMCC), dedicated to the development and establishment of an industry-standard interface specification for Hybrid Memory Cube (HMC) technology, today announced the finalization and public availability of its HMCC 2.0 specification (HMCC 2.0).

The new HMCC 2.0 specification advances data rate speeds from 15 Gb/s up to 30 Gb/s, establishing a new threshold for memory performance. HMCC 2.0 also migrates the associated channel model from short reach (SR) to very short reach (VSR) to align with existing industry nomenclature.

"With 150 members, the Hybrid Memory Cube Consortium has gained considerable momentum since its inception and, as a result, has more and better inputs on how the interface can best fit tomorrow's applications," said Jim Handy, director, Objective Analysis. "The release of the HMCC 2.0 specification shows a commitment to evolving a family of specifications targeting all high-performance computing applications."

The HMCC was founded in October 2011 by co-developers Altera, Micron, Open-Silicon, Samsung Electronics and Xilinx. The HMCC finalized and released its first specification in May 2013, demonstrating consensus among leading semiconductor developers to drive adoption of HMC into next-generation systems. Since its establishment, the HMCC has grown to include more than 150 OEMs, enablers and integrators who regularly participate in the development and discussion of HMC standards. Finalization of the second generation of HMCC specifications is a key milestone in the development of this innovative memory technology and an indication of its continued adoption.

"HMCC 2.0 gives designers a mature solution for breaking through memory bottlenecks and delivering a new generation of systems with unprecedented memory performance," said Hans Boumeester, Open-Silicon's vice president of IP and engineering operations. "Ratification of the new standard means that these designers will have access to standards-compliant IP for immediate integration into chips and systems that meet the growing bandwidth demands of next-generation data center and high-performance computing applications."

About HMC

HMC, which has been recognized by industry leaders and influencers as the long-awaited answer to address the limitations imposed by conventional memory technology, provides ultra-high system performance with significantly lower power per bit. The current generation of HMC technology delivers up to 15 times the bandwidth of a DDR3 module and uses 70 percent less energy and 90 percent less space than such technologies. HMC's abstracted memory allows designers to devote more time to leveraging HMC's revolutionary features and performance and less time navigating the multitude of memory parameters required to implement basic functions. It also manages error correction, resiliency, refresh and other parameters exacerbated by memory process variations.

About the HMCC

Founded by leading members of the world's semiconductor community, the Hybrid Memory Cube Consortium is dedicated to the development and establishment of an industry-standard interface specification for the Hybrid Memory Cube technology. Members of the consortium include Altera Corporation, ARM, IBM, Micron Technology, Inc., Open-Silicon, Inc., Samsung Electronics Co., Ltd., SK hynix Inc., and Xilinx, Inc. To learn more about the HMCC, visit www.hybridmemorycube.org.

CONTACT: Karl Stetson

Zeno Group for Micron

Karl.stetson@zenogroup.com

206-297-5943



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