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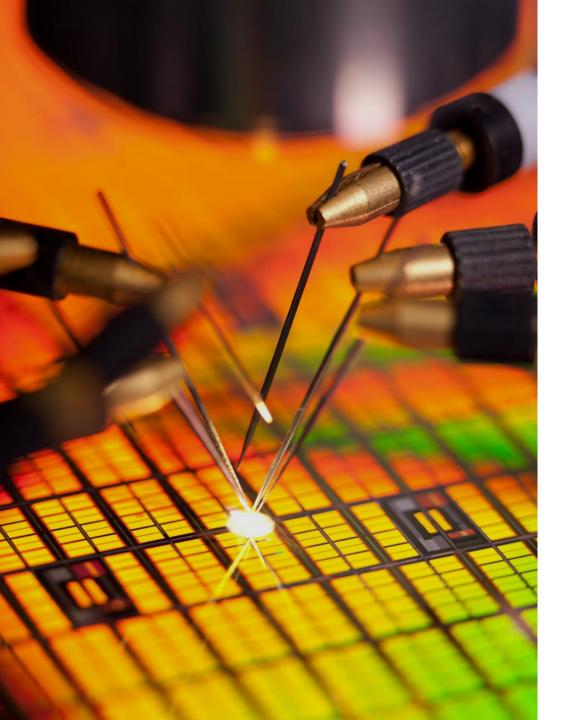
Accelerating Memory and Storage Innovation

Scott DeBoer, Executive Vice President

2019 Analyst & Investor Webcast | May 2019

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Agenda

Team

Core Technology

Execution



Team

Core Technology
Execution



Industry's Best Talent

Getting Even Stronger

Team

Strong and Getting Stronger

Global talent fuels innovation

Top 50 on US Patent list

Forbes 2019 "The Best Employer for Diversity" list

New Talent

Attracting the World's Best

>50% of R&D new hires with MS, PhD >60% technical with industry experience Certified 2018 Great Place to Work

Pipeline

Advancing STEM Education

Advancing Curiosity grants

Promoting STEM education

Engaged with top global universities



Global Technology Development

Delivering World Leading Innovation and Execution



Core R&D Idaho, U.S.

Accelerate Core Technology with Disruptive Innovation



DRAMJapan



NANDSingapore



3D XPointTM Utah, U.S.



Packaging Taiwan

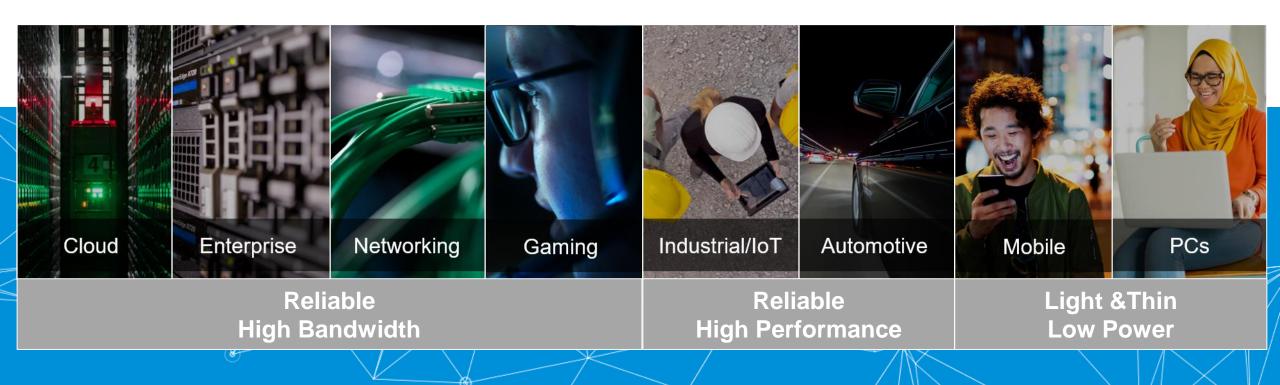


Automotive Virginia, U.S.

Strong Development Capability at Manufacturing Locations



Core Technology Delivering Across Spectrum of Customer Needs







Team

Core Technology

Execution





Core Technology DRAM Micron 10

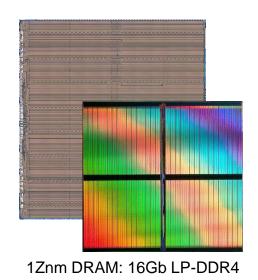
1Znm DRAM

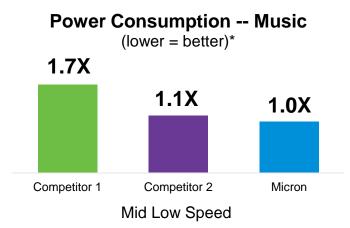
Continuing Rapid Improvement in Competitive Position

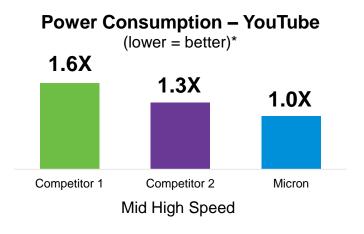
Industry leading mobile 16Gb

Rapid progress on 1Znm yield ramp

Strengthening competitive position





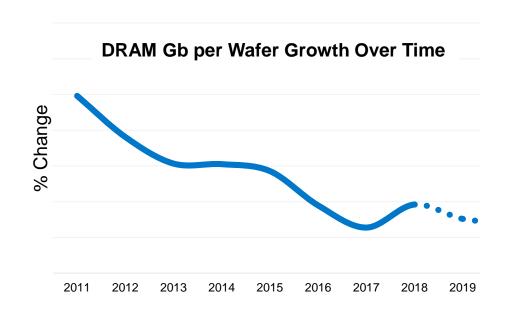


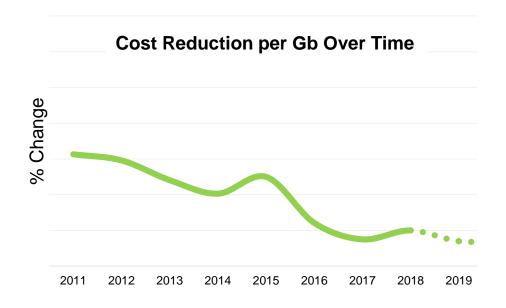


DRAM Scaling Trends

DRAM Scaling Challenges Evident in Industry Trends

Gb/Wafer increases significantly more difficult
Cost of node transitions challenging ultimate benefits
Capex Intensity continues to grow

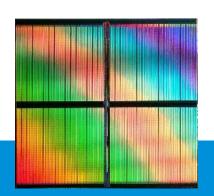




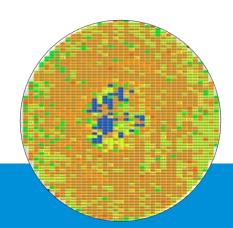


DRAM Scaling: Driving Towards Technology Leadership

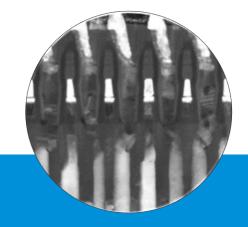
Continuing to Extend Roadmap for Cost and Performance Improvement



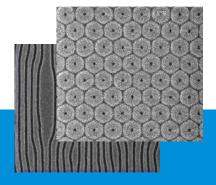
Customer Qualification



1 C Yield Improvement



1 B Early Process Integration



1 Y Architectural Pathfinding

Technology roadmap extending

Difficult physics and cost challenges beyond 1β

Node transition value evolution



Optimized Approach to Lithography

Multiple Patterning Technology Optimized for Micron Future DRAM Nodes

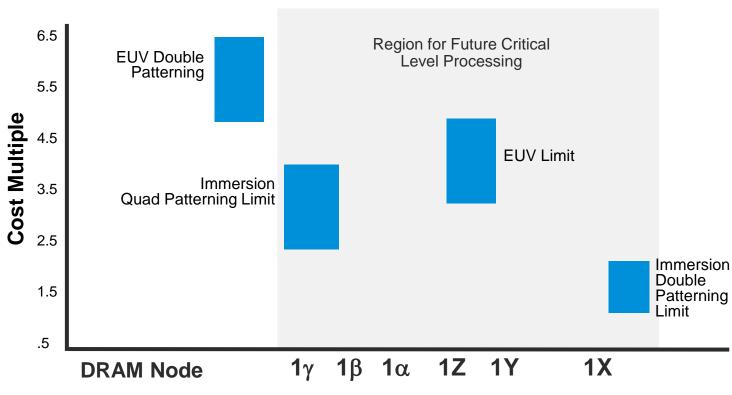
Micron's pattern multiplication technology is a strategic advantage

Proven technology capability and cost efficiency for 1Znm through 1γnm

Ongoing evaluation of EUV Lithography for DRAM

Prepared for implementation of EUV when beneficial to Micron

Cost Compared to Immersion



Lithography technology breakpoints & relative costs



Optimized Approach to Lithography

EUV Patterning Challenges for Advanced DRAM Applications

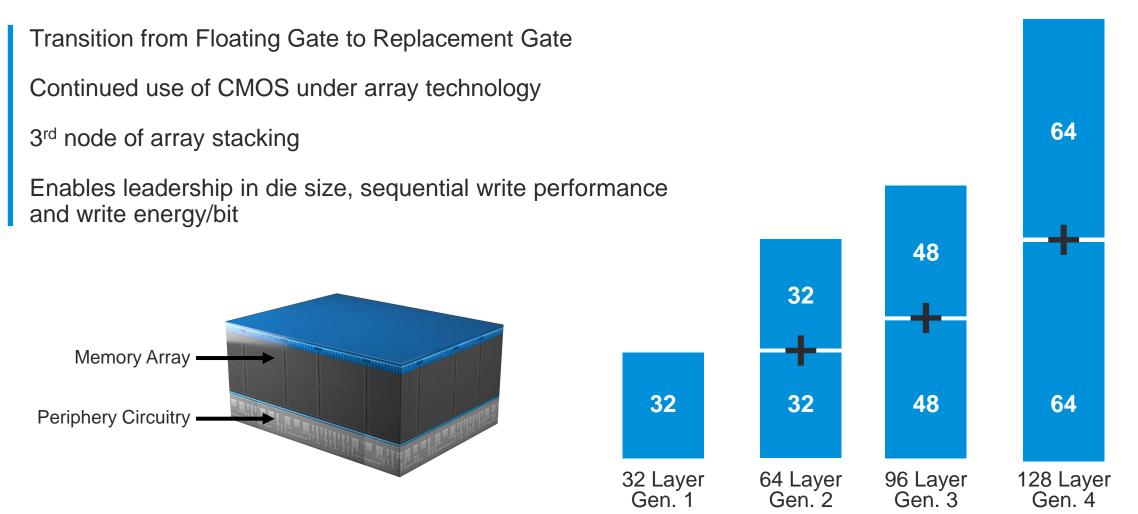
		Uniformity (Local Variation)	Cost Competitiveness (\$ per Wafer)
DRAM 1Znm → 1αnm	Immersion Multi Patterning		
	EUV Single Exposure <i>Optimal Dos</i> e		
DRAM beyond 1αnm	Immersion Multi Patterning		
	EUV Single Exposure <i>High D</i> ose		
	EUV Single Exposure <i>Low D</i> ose		



Core Technology NAND Micron[®] 16

128 Layer NAND

Solid Progress on Replacement Gate Technology Provides Confidence for Transition

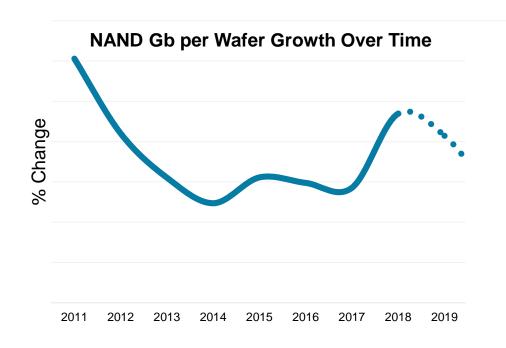


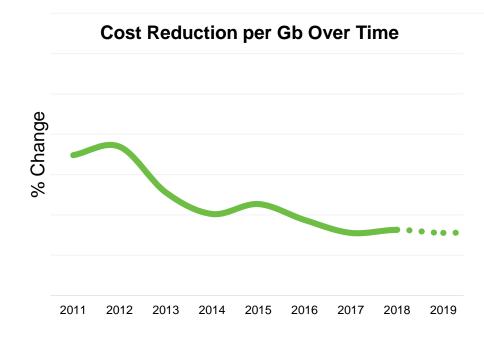


NAND Scaling Trends

Node to Node Benefits Reducing Post 3D NAND Transition

Substantial increase in Gb/wafer driven by planar to 3D conversion Gb/wafer growth slows beyond the 64 layer transition Industry rate of cost reduction leveling off

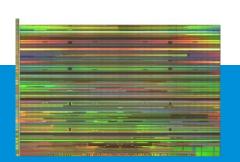




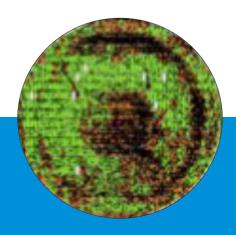


NAND Scaling: Leadership Through Technology Transition

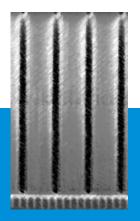
Delivering World Leading Cost and Performance



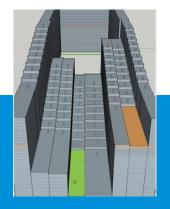
96 Layer FG Mature Yield



128 Layer RGYield Improvement



1YY Layer RG
Early Process Integration



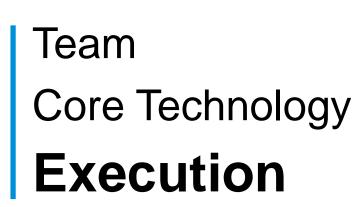
2XX Layer RGArchitectural Pathfinding

RG technology transition primary focus

Density increases and cost reductions slowing

Driving towards cost and performance leadership





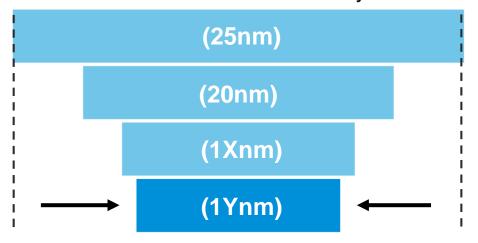


Delivering Faster Yield Ramps

Time to Mature Yield Reduced by More than Half

DRAM

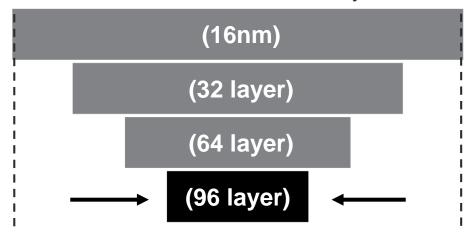
Time to Mature Yield Reduced by >50%



Time to Mature Yield

NAND

Time to Mature Yield Reduced by > 65%



Time to Mature Yield

Source: Micron



Driving our performance to a still higher level.



Team



Technology



Execution



