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Convey Computer Introduces Innovative Computer Architecture for Big Data

-- Smarter Design of MX System Brings Performance and Affordability to Large, Hard to Partition Problems --

Richardson, Texas—November 12, 2012—Convey Computer™ Corporation announced today a new computer architecture—the MX™ Series—that directly addresses the computing needs of high-performance analytics applications.

Big data analytics, like those found in genomics, graph analytics, social network analytics, fraud detection, and security are typically not well suited for racks of commodity systems. These types of applications demand a new approach to computing that brings performance and affordability to solving extremely large, irregular and hard to partition problems. The Convey MX Series is a smarter computer architecture tailored to meet this growing need.

The new Convey architecture features the capability to run tens of thousands of threads of execution coupled with a smart memory system that can atomically perform “in-memory” arithmetic operations. Architected to scale up to 32 terabytes of physical memory, the MX Series can exploit massive degrees of parallelism while efficiently handling hard-to-partition algorithms.

To enhance development productivity, the MX offers a new suite of compilers and tools built on OpenMP giving users access to today’s most pervasive parallel programming model. A unique runtime thread library takes advantage of hardware based scheduling that avoids the scaling bottlenecks typical of traditional thread scheduling mechanisms—enabling efficient scaling on the MX Series.

“Many high performance analytics (HPA) applications are organized around pointer-based data structures, such as trees and graphs. These irregular applications are hard to partition and generally run inefficiently on commodity clusters,” explained Bruce Toal, CEO of Convey. “The MX Series successfully solves this challenge with an

innovative architecture uniquely packaged in a high-performance, power-efficient, and affordable solution.”

Analyst firm IDC expects the use of Big Data methods will soon become a requirement for competitiveness in a broad range of market sectors. “Standard clusters by themselves are not designed to efficiently handle some of the most challenging, high-value work, especially graph analytics and other hard-to-partition problems,” explains Steve Conway, Research Vice President of IDC's High Performance Computing Group. “Convey’s unique approach is designed to excel at tackling the data-level parallelism (DLP) that characterizes many of these problems. Convey’s hybrid-core solutions target better time efficiency, power efficiency, and cost efficiency—not to mention the ability to obtain answers that would be impractical without high-performance analytics.”

The MX Architecture complements Convey’s existing HC Series by increasing memory features and parallelization capabilities. Both architectures provide a robust platform for researchers developing high performance analytics (HPA) applications. In many situations, Convey hybrid-core systems can replace tens or hundreds of commodity systems dedicated to HPA applications. Using the Convey hybrid-core systems, customers can dramatically accelerate a wide range of applications, while lowering energy consumption.

About Convey Computer Corporation

Convey systems break power, performance and programmability barriers with the world’s first hybrid-core computer—a system that marries the low cost and simple programming model of a commodity system with the performance of a customized hardware architecture. Using the Convey hybrid-core systems, customers worldwide in industries such as life sciences, research, big data, and the government/military are enjoying order of magnitude performance increases.

For More Information:

At SC12, please visit Convey in booth #2001 or contact Bob Masson, Convey’s director of product marketing, at 720-352-5157 (mobile) or email bmasson@conveycomputer.com.

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