



February 25, 2014

Hybrid Memory Cube Consortium Continues to Drive HMC Industry Adoption With Release of Second-Generation Specification

Initial Draft of Gen2 Spec Released

SAN JOSE, Calif. and BOISE, Idaho, Feb. 25, 2014 (GLOBE NEWSWIRE) -- The Hybrid Memory Cube Consortium (HMCC), dedicated to the development and establishment of an industry-standard interface specification for the Hybrid Memory Cube (HMC) technology, today announced its continued work to build the HMC ecosystem and support for the industry adoption of this groundbreaking technology through the development of a new interface specification. Today the HMCC also released a first draft of the new specification to a growing list of consortium adopters that now numbers more than 120. The new specification supports increased data rate speeds advancing short-reach (SR) performance from 10 Gb/s, 12.5 Gb/s, and 15 Gb/s, up to 30 Gb/s. The new specification also migrates the associated channel model from SR to VSR to align with existing industry nomenclature. The ultra short-reach (USR) definition also increases performance from 10 Gb/s up to 15 Gb/s.

The HMCC, founded by leading memory providers Micron Technology (Nasdaq:MU), Samsung Electronics, and SK hynix, has begun circulating this draft specification to a broad range of adopters, with the goal of incorporating adopter members' input and targeting a completion date of May 2014 for the final version. The first-generation specification was completed and released publicly in April 2013; several developer and adopter companies, including Altera, Xilinx, and Open-Silicon, have already begun leveraging the specification to design products and solutions that incorporate HMC technology.

"Using the HMC Gen2 specification, designers can extract even more performance from our UltraScale FPGA architecture," said Hugh Durdan, vice president of portfolio & solutions marketing at Xilinx. "Our UltraScale devices, which are currently shipping, were designed to support this specification and offer lower risk and faster time to market for high-bandwidth applications."

"The HMC Gen2 specification doubles the interface data rate, which enables system designers to more easily realize performance gains with next-generation 20nm and 14nm FPGAs and SoCs," said Patrick Dorsey, senior director of product marketing at Altera. "Our early start in delivering evaluation boards and the demonstrated interoperability between Hybrid Memory Cube devices and FPGAs enables customers to immediately start evaluating and developing HMC-based, high-performance systems."

The consortium is a focused collaboration of OEMs, enablers and integrators who are codeveloping and implementing an open interface standard for HMC, a high-performance memory solution developed by Micron. Developer members Micron Technology, Inc., Samsung Electronics Co., Ltd., Altera Corporation, ARM, IBM, Open-Silicon, Inc., SK hynix, Inc., and Xilinx, Inc., are working directly with adopters to support collective requirements for the creation of new markets and industry adoption of HMC.

An industry breakthrough, HMC uses advanced through-silicon vias (TSVs)—vertical conduits that electrically connect a stack of individual chips—to combine high-performance logic with dynamic random access memory (DRAM) die. The first commercial HMC implementation is sampling from Micron in a 2GB density with an unprecedented 160 GB/s of memory bandwidth, while using up to 70 percent less energy per bit than existing technologies, which dramatically lowers customers' total cost of ownership.

HMC has been recognized by industry leaders and influencers as the long-awaited answer to the growing gap between the performance improvement rate of DRAM and processor data consumption rates. HMC capabilities represent a leap beyond current and near-term memory architectures in the areas of performance, packaging, and power efficiencies, offering a major shift from present memory technology.

Become an HMCC Member

Adopter membership in the HMCC is available to any company interested in participating in the development of HMC specifications. Additional information, technical support specifications and other tools for adopting the technology can be found at www.hybridmemorycube.org.

About the HMCC

Founded by leading members of the world's semiconductor community, the Hybrid Memory Cube Consortium (HMCC) is dedicated to the development and establishment of an industry-standard interface specification for Hybrid Memory Cube technology. Members of the consortium include Altera, ARM, IBM, Micron Technology, Open-Silicon, Samsung., SK hynix and Xilinx. To learn more about the HMCC, visit www.hybridmemorycube.org.

CONTACT: Mary Ellen Ynes

Zeno Group for Micron

+1.650.801.7954

maryellen.ynes@zenogroup.com

John Lucas

Samsung Electronics Co., Ltd.

+1.408.544.4363

j.lucas@ssi.samsung.com